REMARKS

Upon entry of the above amendment, claims 1, 16 and 27 will have been amended. Support for the amendment to claims 1, 16 and 27 can be found on e.g., page 7, lines 8-15. No new matter has been added. Accordingly, claims 1-22 and 27 will be pending with claims 1, 16 and 27 being in independent form. Reconsideration of the Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Present Amendment is proper for entry

Applicants respectfully submit that the instant amendment is proper for entry after final rejection. Applicants note that no question of new matter is presented nor are any new issues raised in entering the instant amendment of the claims and that no new search would be required. Moreover, Applicants submit that the instant amendment places the application in condition for allowance, or at least in better form for appeal. Accordingly, Applicants request the Examiner to enter the instant amendment, consider the merits of the same, and indicate the allowability of the present application and each of the pending claims.

Rejection Under 35 U.S.C. § 102(b)

Claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17 and 21 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent No. 6,399,970 to KUBO et al. This rejection is

respectfully traversed.

The Examiner asserts that KUBO discloses forming each of the recited channels in the substrate and providing the recited layers therein. Applicants respectfully disagree.

Notwithstanding the Office Action assertions as to what KUBO discloses, Applicants submit that, in addition to the reasons already made of record, KUBO clearly fails to disclose, or even suggest, for example, forming, *by removing material from an upper surface of a substrate,* a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel in the substrate (claim 1). KUBO also fails to disclose, or even suggest, forming a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel *by etching an upper surface* of a substrate (claim 16).

Applicants acknowledge that KUBO discloses a substrate 10 upon which pFET and NFET channels are formed. KUBO also discloses arranging layers 14n within the channels and that the "layer 14n and the Si layer 13n immediately therebelow are fitted in lattice for each other" (see col. 8, lines 51-53). Finally, KUBO discloses, at col. 10, lines 51-57, "that the lattice misfit of the SiGeC layer 14n with respect to the Si substrate is zero ..." However, it is clear that the channels for the nFET and the pFET are formed in successively formed layers built up on the substrate 10 and that it is only the trench isolation that is formed by material removal or etching of the upper surface of the substrate 10 (see figures and e.g., col. 9, lines 46-50). The invention, as exemplified by Applicants' Fig. 1c, provides for forming channels 40 and 45 in the substrate 20 by material removal and/or etching of the substrate.

Thus, Applicants submit that the above-noted claims are not disclosed, or even suggested, by any proper reading of KUBO.

Furthermore, Applicants submit that dependent claims 2, 4, 6, 7, 9, 10, 12, 17 and 21 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicants submit that no proper reading of KUBO discloses or even suggests, in combination:

(i) a first layer of Si:C;

(ii) a Ge content of greater than 25%; and

(iii) a stress component of greater than 3 GPa.

Applicants respectfully request that the rejection of the above-noted claims be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 3, 11, 18 and 22 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of U.S. patent 6,790,699 to VOSSENBERG et al. Claims 5, 13 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO alone. Claims 8, 19, 20 and 27 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of U.S. patent 5,683,934 to CANDELARIA. Claim 14 was rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of pages 256-257 of Silicon Processing for the Vlsi Era, Vol. 1: Process Technology, Second Edition, by Stanely WOLF et al. These rejections are respectfully traversed.

The Examiner acknowledged that KUBO lacks, among other things, the separate

forming of the pFET and nFET channels, the recited tensile stress value, a first layer of material that is Si:C, and a substrate that is silicon on insulator. However, the Examiner asserted that VOSSENBERG discloses the separate forming of the channels and that the recited tensile stress values would have been obvious on the basis of the teachings of KUBO alone. The Examiner further asserts that CANDELARIA teaches the use of carbon-doped silicon channel within a p-channel, and that WOLF teaches the silicon on insulator substrate. The Examiner also concludes that it would have been obvious to modify KUBO so as to render the features recited in the above-noted claims obvious to one of ordinary skill in the art. Applicants respectfully traverse each of the above-noted rejections.

Notwithstanding the Office Action assertions as to what each of the above-noted documents disclose or suggest, Applicants submit that no proper combination of the above-noted documents discloses or suggests, for example, forming, *by removing material from an upper surface of a substrate,* a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel in the substrate (claim 1), and/or forming a p-type field-effect-transistor (PFET) channel and a n-type field-effect-transistor (nFET) channel *by etching an upper surface* of a substrate (claim 16), and/or *etching into an upper layer of a substrate* a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel (claim 27).

As explained above, Applicants do not dispute that KUBO discloses a substrate 10 upon which pFET and NFET channels are formed. KUBO also apparently discloses arranging layers 14n within the channels and that the "layer 14n and the Si layer 13n immediately therebelow are fitted in lattice for each other" (see col. 8, lines 51-53).

Finally, KUBO discloses, at col. 10, lines 51-57, "that the lattice misfit of the SiGeC layer 14n with respect to the Si substrate is zero ..." However, it is clear that the channels for the nFET and the pFET are formed in successively formed layers built up on the substrate 10 and that it is only the trench isolation between the nFET and the pFET that is formed by material removal or etching of the upper surface of the substrate 10 (see figures and col. 9, lines 46-50). The invention, as exemplified by Applicants' Fig. 1c, provides for forming channels 40 and 45 in the substrate 20 by material removal and/or etching of the substrate.

Applicants notes that VOSSENBERG merely discloses the manuafucturing process for a sensor using surface micromachining (see col. 3, lines 36-41). VOSSENBERG, however, lacks any disclosure with regard to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel. Nor has the Examiner identified any language in VOSSENBERG which discloses of suggests this feature.

Applicants do not dispute that CANDELARIA discloses a channel layer 12 which comprises carbon-doped silicon (see col. 3, lines 45-50). CANDELARIA, however, does not disclose or suggest the features recited in 8, 19 and 20 in combination with the features recited in claims 1, 16 and 27. Indeed, CANDELARIA specifically lacks any disclosure with regard to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET

channel (claims 1, 16 and 27). Nor has the Examiner identified any language in CANDELARIA which discloses of suggests these features.

With regard to WOLF, Applicants submit that this document merely discloses that "[s]ilicon on insulator technology has been available since the late 1960's" (see page 256). WOLF, however, does not disclose or suggest the features recited in claim 14 in combination with the features recited in claim 1. Indeed, WOLF specifically lacks any disclosure with regard to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel. The Examiner has not identified any language in WOLF which discloses of suggests this feature.

Additionally, Applicants submit that there is no motivation to modify KUBO in view of VOSSENBERG, CANDELARIA, and WOLF or in a manner which would render obvious Applicants' invention, and additionally, Applicants submit that there is no motivation or rationale disclosed or suggested in the prior art to modify the applied references in the manner suggested by the Examiner.

Applicants further submit that dependent claims 3, 5, 8, 11, 13-15, 18-20 and 22 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicants submit that no proper combination of KUBO, VOSSENBERG, CANDELARIA, and WOLF discloses or even suggests, in combination:

A) the features recited in claims 3, 5, 8, 11 and 13-15 in combination with the features recited in claim 1 such as:

(i) the separate forming of the pFET and nFET channels;

(ii) the tensile stress in the epitaxial semiconductor layer being greater than 3 GPa;

(iii) the Si:C first layer;

(iv) forming the first and second layers with a hard mask over the pFET and nFET channels;

(v) the first and second layer heights of between about 100 Å and 300 Å;

(vi) the silicon on insulator; and

(vii) the Ge percentage of between 25% and 30%.

B) the features recited in claims 18-20 in combination with the features recited in claim 16 such as:

(i) the separate forming of the pFET and nFET channels;

(ii) the Si:C first layer and the SiGe second layer; and

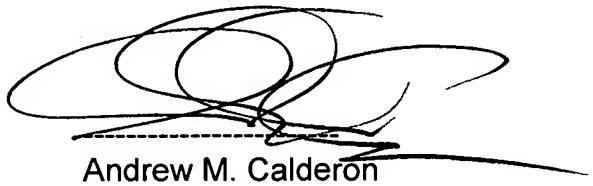
(iii) the compressive stress in the pFET channel and the tensile stress in the nFET channel.

Applicants respectfully request that the above-noted rejections of the above-noted claims be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that the claims are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue, and to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **Deposit Account No. 09-0458**.

Respectfully submitted,
D. CHIDAMBARRAO et al.



Andrew M. Calderon
Reg. No. 38,093

October 24, 2005
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
703-716-1191